F28M35H20B1, F28M35H20C1, F28M35H22B1, F28M35H22C1, F28M35H32B1, F28M35H32C1, F28M35H50B1, F28M35H50C1, F28M35H52B1, F28M35H52C1 Concerto MCU

Silicon Errata

Literature Number: SPRZ357B
August 2011–Revised January 2012

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F28M35x Concerto MCU Silicon Errata

1 Introduction

This document describes the silicon updates to the functional specifications for the F28M35x microcontrollers (MCUs).

The updates are applicable to:

- 144-pin PowerPAD™ Thermally Enhanced Thin Quad Flatpack, RFP Suffix

2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all Concerto™ MCU devices and support tools. Each Concerto™ MCU commercial family member has one of three prefixes: x, p, or no prefix (e.g., **x**F28M35H52C1RFPT). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with prefix **x**/TMDX) through fully qualified production devices/tools (no prefix/TMDS).

xF28M35...	Experimental device that is not necessarily representative of the final device's electrical specifications
pF28M35...	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
F28M35...	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing
TMDS	Fully qualified development-support product

Devices with prefix **x** or **p** and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices with prefix of **x** or **p** have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RFP) and temperature range (for example, T).

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3 Device Markings

Figure 1 provides an example of the Concerto device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 1. Some prototype devices may have markings different from those illustrated. Figure 2 shows an example of the device nomenclature.

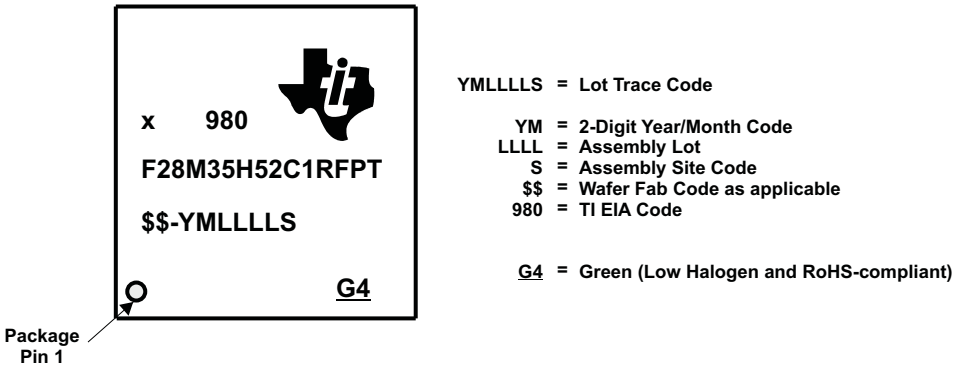
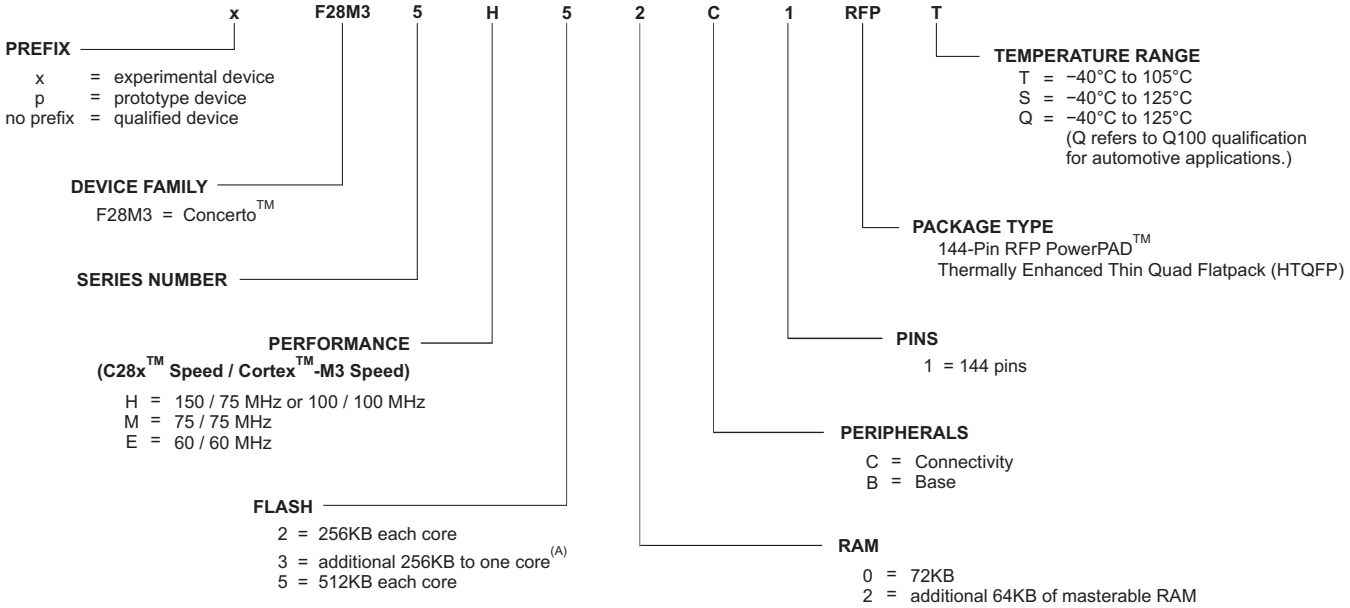


Figure 1. Example of Device Markings

Table 1. Determining Silicon Revision From Lot Trace Code

SECOND LETTER IN PREFIX OF LOT TRACE CODE	SILICON REVISION	REVISION ID	COMMENTS
Blank (no second letter in prefix)	Indicates Revision 0	Cortex™-M3: 0x400F EC00 C28x™: 0x0883	This silicon revision is available as **x** (experimental device).
		0x0000	


x F28M3 5 H 5 2 C 1 RFP T
PREFIX
x = experimental device
p = prototype device
no prefix = qualified device
DEVICE FAMILY
F28M3 = Concerto™
SERIES NUMBER
PERFORMANCE
(C28x™ Speed / Cortex™-M3 Speed)
H = 150 / 75 MHz or 100 / 100 MHz
M = 75 / 75 MHz
E = 60 / 60 MHz
FLASH
2 = 256KB each core
3 = additional 256KB to one core(A)
5 = 512KB each core
RAM
0 = 72KB
2 = additional 64KB of masterable RAM
PERIPHERALS
C = Connectivity
B = Base
PINS
1 = 144 pins
PACKAGE TYPE
144-Pin RFP PowerPAD™
Thermally Enhanced Thin Quad Flatpack (HTQFP)
TEMPERATURE RANGE
T = −40°C to 105°C
S = −40°C to 125°C
Q = −40°C to 125°C
(Q refers to Q100 qualification for automotive applications.)

A The additional 256KB is added to the Cortex™-M3 core (Connectivity Devices) or to the C28x™ core (Base Devices).

Figure 2. Example of Device Nomenclature

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4 Known Design Marginality/Exceptions to Functional Specifications

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NOTE: For errata relating to the Cortex™-M3 r2p0 core, see the *ARM Core Cortex-M3 / Cortex-M3 with ETM (AT420/AT425) Errata Notice* at the ARM® Ltd. website.

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Advisory — *Debug: Global Run of Cortex™-M3 and TMS320C28x™ is not Operational*

Revision(s) Affected 0

Details Due to missing signals in the debug logic, global run of the Cortex™-M3 and C28x™ cores is not enabled.

Workaround(s) None. This will be fixed in the next revision of the silicon.

Advisory — *Debug: Cross-Trigger Functionality is Limited When Using Breakpoints on the C28x Core*

Revision(s) Affected 0

Details When cross-triggering is enabled, halting at a breakpoint set for the C28x core does not also halt the Cortex™-M3 core.

Workaround(s) None

Advisory — *Debug: Control Subsystem Boot ROM M0 RAM-INIT Does Not Wait for RAM-INIT to Complete*

Revision(s) Affected 0

Details C-Boot-ROM sets the RAM-INIT bit to zero-initialize the entire M0 RAM every time it is run after reset. However, it does not wait for the RAM-INIT to complete before accessing M0 RAM for run-time stack. This does not cause any problem on stand-alone device operation because this wait before RAM is accessed is inherently achieved by the wait to access Flash. As Flash power-up time is more than the M0 RAM-INIT time and the Boot ROM waits for Flash to power up completely before accessing RAM, by the time C-Boot-ROM accesses M0 RAM for stack, it is initialized properly.

Workaround(s) On stand-alone device operation, this is not a problem because every time the device is reset, Flash has to be brought back to active state and this wait for Flash to come to active state is more than the time required for M0 RAM-INIT to complete.

During debug/development, when the emulator is connected and the user wants to RUN through Boot ROM, care must be taken to ensure that Flash is not accessed before running through boot initialization or the user should carefully step through Boot ROM code at least until RAM-INIT is done, before clicking the RUN button on CCS.

This will be fixed in the next revision of the silicon.

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Advisory — *NMI: Writing a "0" to Any of the CNMIFRC/MNMIFRC Register Bits Clears the Corresponding Flag Bit in CNMIFLG/MNMIFLG*

Revision(s) Affected 0

Details Writing a "0" to any of the bits in the Control Subsystem CNMIFRC register clears the corresponding bits in the CNMIFLG register. Likewise, writing a "0" to any of the bits in the Master Subsystem MNMIFRC register clears the corresponding bits in the MNMIFLG register.

Workaround(s) Do not write "0" to any of the bits in the CNMIFRC register or MNMIFRC register. To clear the CNMIFLG and MNMIFLG bits, write a "1" to the corresponding bits in the respective CNMIFLGCLR and MNMIFLGCLR registers.

This will be fixed in the next revision of the silicon.

Advisory — *PLL: Setting SYSPLLMULT or UPLLMULT to 0x0000 causes "/0" Condition in PLL Logic*

Revision(s) Affected 0

Details Setting the SYSPLLMULT register or UPLLMULT register to 0x0000 to bypass the PLL causes a "/0" condition in the PLL logic and results in an unstable PLL output clock.

Workaround(s) Do not write 0x0000 to the SYSPLLMULT register or UPLLMULT register to bypass either PLLs. Instead, to bypass the system PLL, set SYSPLLCTL[SPLLCLKEN] = 0. To bypass the USB PLL, set UPLLCTL[UPLLCLKEN] = 0.

This will be fixed in the next revision of the silicon.

Advisory — *USB: VBUS Pin May Clamp to 3.3-V Supply, Preventing Proper OTG Mode Operation*

Revision(s) Affected 0

Details The VBUS pin may clamp to V_{DDIO}, preventing the pulldown resistors from taking effect in USB-OTG mode when attempting to end a session.

Workaround(s) None

Advisory — *USB: Host Mode — Cannot Communicate With Low-Speed Device Through a Hub*

Revision(s) Affected 0

Details When the USB controller is operating as a Host and a low-speed packet is sent to a device through a hub, the subsequent Start-of-Frame is corrupted. After a period of time, this corruption causes the USB controller to lose synchronization with the hub, which results in data corruption.

Workaround(s) None

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Advisory

Control Subsystem: Reset Value (/8) of CCLKCTL.CLKDIV Bit Field Violates the MIN Requirement Mandated by the Data Manual for ACIBCLK, When the Input Clock to the Divider is Less Than 40 MHz

Revision(s) Affected

0

Details

On power up or after an external reset ($\overline{\text{XRS}}$), PLL is bypassed and the Master Boot ROM configures the default SYSCLK divider to "/1". This makes the input clock to the divider the same as OSCCLK. If OSCCLK is less than 40 MHz, then upon power up or an external reset, ACIBCLK would be less than 5 MHz. However, this is not an issue because the Analog Subsystem needs not be functional during boot time.

Workaround(s)

An OTP function is provided in the Control Subsystem for users to call during their application initialization process and before using Analog Subsystem peripherals on the device. This function will configure the CCLKCTL divider as needed by the application.

This will be fixed in the next revision of the silicon.

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Advisory — *Master Subsystem: MNMIFLG.NMIINT Bit Will Not be Set in Some Cases When an NMI is Still Pending*

Revision(s) Affected 0

Details On the Master Subsystem, if there is a nested NMI and if the user clears the MNMIFLG.NMIINT bit before clearing all the other pending flags while returning from the first NMI handler, then the MNMIFLG.NMIINT bit will not be set while the second NMI is still pending. This pending NMI will keep the MNMIWD counter running and will reset the device if the pending flag is not cleared on time.

If the second NMI among the nested NMI is a Missing-clock NMI, then immediately after MNMIWD reset, there will be another NMI because of the MCLKSTS bit being set.

Workaround(s) User NMI handler should not depend on the MNMIFLG.NMIINT bit to determine if there is an active NMI pending and should instead look at all the individual bits to check if an NMI is pending.

This will be fixed in the next revision of the silicon.

Advisory — *Master Subsystem I2C: Data Hold Time Violates Philips® I2C Specification*

Revision(s) Affected 0

Details The Master subsystem I2C module's data hold time on F28M35x Concerto devices is a minimum of 2 system clock cycles, which violates the Philips® I2C specification requirement of a minimum of 0 system clock cycle.

Workaround(s) None

Advisory — *Master Subsystem MPU: Memory Protection Unit is Disabled*

Revision(s) Affected 0

Details The Cortex™-M3 Memory Protection Unit (MPU) is disabled on the F28M35x Revision 0 silicon.

Workaround(s) None. This will be fixed on the next revision of the silicon.

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Advisory — *Master Subsystem Boot ROM: NMI Handler Can Return Before Clearing All the Pending NMIs, if There is a Nested NMI*

Revision(s) Affected 0

Details The Master Subsystem Boot ROM depends on the MNMIFLG.NMIINT bit to determine if there is a pending NMI on the Master Subsystem. However, as mentioned in the advisory titled "Master Subsystem: MNMIFLG.NMIINT Bit Will Not be Set in Some Cases When an NMI is Still Pending", this bit might not be set. Therefore, the Master Boot ROM NMI handler might return while there is an active NMI pending and MNMIWD counter running. This will trigger MNMIWDRST and reset the entire device. The probability of nested NMI happening during boot time is highly unlikely, unless there is a critical issue elsewhere in the device.

Workaround(s) None. This will be fixed in the next revision of the silicon.

Advisory — *Master Boot ROM: NMI Handler Not Executed if NMI Occurs at Power Up or Immediately After a Reset*

Revision(s) Affected 0

Details If there is an NMI at power up or immediately after a reset, the master Boot ROM will branch to the NMI handler. Since access to all memories is blocked upon reset, the NMI handler will not be able to acknowledge the NMI, which will cause the MNMIWD counter to eventually overflow and reset the device. If this NMI is a missing clock NMI, there will be another NMI after the MNMIWD reset because the MCLKSTS bit is not cleared by an external (or watchdog) reset. Therefore, if there is a missing clock condition upon power up or immediately after an external reset, then the device will keep resetting over and over again.

Workaround(s) None. This will be fixed in the next revision of the silicon.

Advisory — *Master Boot ROM: Parallel Boot Mode Will Not Work as Intended*

Revision(s) Affected 0

Details Parallel boot mode does not transfer data into the device in the intended format.

Workaround(s) Use ARM® production programming solutions for Cortex™-M3 programming.

This will be fixed in the Boot ROM in the next revision of the silicon.

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Advisory	***GPIO: GPIOs on Port C Do Not Toggle Correctly When Using the GPCTOGGLE Register***
Revision(s) Affected	0
Details	GPIOs on Port C do not toggle correctly when using the GPCTOGGLE register because of a dependency on the state of GPIOs on Port A.
Workaround(s)	Use GPCSET and GPCCLEAR registers or the GPCDAT register to toggle Port C GPIOs. This will be fixed in the next revision of the silicon.

Advisory	***C28x Flash: Code Executing From the C28x Subsystem Flash May be Subject to Unnecessary 1-Cycle Delays***
Revision(s) Affected	0
Details	Code executing from the C28x Subsystem Flash may be subject to unnecessary 1-cycle delays. This delay will not occur more often than once every 8 instructions for code that is composed of linear 32-bit opcodes with no pipeline delays (worst case). In practice, the unnecessary delay occurs rarely since the C28x uses both 16-bit opcodes and 32-bit opcodes. This delay can occur when Flash wait states are set to "3" and the prefetch mechanism is enabled. This delay does not occur when the wait states are set to "2" or "1" with prefetch enabled.
Workaround(s)	None. This will be fixed in the next revision of the silicon.

Advisory	***C28x Clocking: EALLOW Protection of C28x Clocking Registers Prevents Read of Registers***
Revision(s) Affected	0
Details	The EALLOW protection of the C28x clocking registers prevents reads to these registers (reads return 0x0000) in addition to preventing writes to the registers (expected behavior of EALLOW-protection) when EALLOW is not set.
Workaround(s)	Prior to reading C28x clocking registers, the application code must first execute the “EALLOW” command. This will be fixed in the next revision of the silicon.

Advisory	***µDMA: No Transfer Completion Interrupt From SW Channels, Other Than Channel 30***
Revision(s) Affected	0
Details	On a Concerto device, if any SW channel, other than Channel 30, is used for data transfer, then there will be no completion interrupt generated on the µDMA interrupt line when data transfer is done.
Workaround(s)	The user must poll for the STATE field of the DMASTAT register of SW channel, used for data transfer, to get set to “0x9” to detect completion of data transfer.

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Advisory — *Read of Clock Control Registers on C28x Memory Map is EALLOW-Protected*

Revision(s) Affected 0

Details Clock Control Registers on the C28x memory map are read-protected by EALLOW.

Workaround(s) Enable EALLOW before reading the Clock Control Registers on the C28x memory map.

Advisory — *VCU: First CRC Calculation May Not be Correct*

Revision(s) Affected 0

Details Due to the internal power-up state of the VCU module, it is possible that the first CRC result will be incorrect. This applies to the first result from each of the eight CRC instructions. This condition can only occur after a power-on reset, but will not necessarily occur on every power on. A warm reset will not cause this condition to reappear.

Workaround(s) The application can reset the internal VCU CRC logic by performing a CRC calculation of a single byte in the initialization routine. This routine only needs to perform one CRC calculation and can use any of the CRC instructions. At the end of this routine, clear the VCU CRC result register to discard the result. An example is shown below.

```
_VCUcrc_reset
MOVZ XAR7, #0
VCRC8L_1 *XAR7
VCRCCLR
LRETR
```

This will be fixed in the next revision of the silicon.

Advisory — *UART: RTRIS Bit in the UARTRIS Register is Only Set When the Interrupt is Enabled*

Revision(s) Affected 0

Details The RTRIS (UART Receive Time-Out Raw Interrupt Status) bit in the UART Raw Interrupt Status (UARTRIS) register should be set when a receive time-out occurs, regardless of the state of the RTIM enable bit in the UART Interrupt Mask (UARTIM) register. However, currently the RTIM bit must be set in order for the RTRIS bit to be set when a receive time-out occurs.

Workaround(s) For applications that require polled operation, the RTIM bit can be set while the UART interrupt is disabled in the NVIC using the IntDisable(n) function in the StellarisWare™ Peripheral Driver Library, where n is 21, 22, or 49, depending on whether UART0, UART1, or UART2 is used. With this configuration, software can poll the RTRIS bit, but the interrupt is not reported to the NVIC.

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Advisory — *Flash ECC: When Program/Data Cache is Enabled, ECC Errors are Captured Only on a Single 64-Bit Slice and Not on the Full 128-Bit Flash Bank Data Width*

Revision(s) Affected 0

Details When the prefetch/cache is enabled using the RD_INTF_CTRL register, ECC is verified only on the 64-bit slice that is requested by the CPU; the other 64-bit slice of the 128-bit Flash bank data width is not verified for ECC errors, and instead, is just loaded into the cache. This is applicable for both Cortex™-M3 and C28x Flash memory modules.

Workaround(s) None

Advisory — *Flash ECC: C28x 'Flash Uncorrectable' Error Generated When Executing F021 Flash API Functions With Flash ECC Enabled*

Revision(s) Affected 0

Details On the Control Subsystem, when Flash ECC is enabled (C28 ECC_ENABLE[ENABLE] = 0xA), execution of any F021 Flash API functions will generate a "Flash Uncorrectable" error and an NMI. Flash ECC is enabled by default.

Workaround(s) Disable C28x Flash ECC before calling F021 Flash API functions by setting C28 ECC_ENABLE[ENABLE] equal to any value other than 0xA. Then, re-enable C28x Flash ECC by setting C28 ECC_ENABLE[ENABLE] equal to 0xA, if desired, after F021 Flash API functions have finished executing.

This will be fixed in the next revision of the silicon.

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Advisory ***VREG: VREG 'Warn Lo/High' Feature Does Not Work as Intended***

Revision(s) Affected 0

Details The VREG "Warn Lo/High" feature should not be used or enabled in the F28M35x Revision 0 devices. Do not set the VREGWARNE bit in the MNMICFG register as it could negatively affect the VREG output voltage.

Workaround(s) None. This will be fixed in the next revision of the silicon.

Advisory ***Temperature Sensor: getTempSlope() and getTempOffset() Functions are not Available on TMX Silicon***

Revision(s) Affected 0

Details The getTempSlope() and getTempOffset() functions are not available for use on TMX silicon.

Workaround(s) None

Advisory ***EMAC: Resetting EMAC Controller Using SRCR2 Register Does Not Automatically Reset the Ethernet PHY Via MII_PHYRST Signal***

Revision(s) Affected 0

Details Resetting the EMAC controller by setting Bit 28 of the SRCR2 register does not automatically reset the Ethernet PHY that is connected to the controller via the MII_PHYRST function on the IO pin.

Workaround(s) The microcontroller signal or pin connected to the Reset pin on the Ethernet PHY should be configured as a GPIO instead of as an MII_PHYRST peripheral pin; and the GPIO must be toggled before resetting the EMAC controller. Toggling the GPIO pin (HIGH → LOW → HIGH) will reset the PHY, assuming the reset for your PHY is an active-**low** signal.

Advisory ***System Control: Clock Configuration Should Not be Changed When There are Pending/On-going Accesses to Shared RAM (Cx and Sx) or to Analog Subsystem***

Revision(s) Affected 0

Details If the clock configuration is being changed (e.g., changing the clock divider for Cortex™-M3) when there is a pending/on-going access to Shared RAM (Cx/Sx) or to the Analog Subsystem, the access could generate an error.

Workaround(s) Software should ensure that there is no pending/on-going access to Shared RAM or to the Analog Subsystem when the clock configuration is being changed.

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Advisory	***RAM Controller: Cortex™-M3 Accesses to Shared RAM (Cx and Sx) and to MSG RAM Do Not Work When Any Other Master (µDMA/C28x/DMA) Simultaneously Accesses the Same Memory***
Revision(s) Affected	0
Details	If Cortex™-M3 accesses Shared RAM (Cx and Sx) or MSG RAM when any other master (µDMA/C28x/DMA) accesses the same memory, data and parity may get corrupted in the memory.
Workaround(s)	When Cortex™-M3 accesses Shared RAM or MSG RAM, no other master (µDMA/C28x/DMA) should access the same memory at that time.

Advisory	***RAM Controller: µDMA Accesses to Shared RAM (Cx and Sx) and to MSG RAM Do Not Work When Any Other Master (Cortex™-M3/C28x/DMA) Simultaneously Accesses the Same Memory***
Revision(s) Affected	0
Details	If µDMA accesses Shared RAM (Cx and Sx) or MSG RAM when any other master (Cortex™-M3/C28x/DMA) accesses the same memory, data and parity may get corrupted in the memory.
Workaround(s)	When µDMA accesses Shared RAM or MSG RAM, no other master (Cortex™-M3/C28x/DMA) should access the same memory at that time.

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5 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: http://www.ti.com.

For further information regarding the F28M35x Concerto devices, see the *F28M35H20B1, F28M35H20C1, F28M35H22B1, F28M35H22C1, F28M35H32B1, F28M35H32C1,F28M35H50B1, F28M35H50C1, F28M35H52B1, F28M35H52C1 Concerto Microcontrollers Data Manual* (literature number SPRS742).

For errata relating to the Cortex™-M3 r2p0 core, see the *ARM Core Cortex-M3 / Cortex-M3 with ETM (AT420/AT425) Errata Notice* at the ARM® Ltd. website.

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6 Revision History

This revision history highlights the technical changes made to the SPRZ357A errata document to make it an SPRZ357B revision.

Scope: See table below.

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Figure 2	Updated "Example of Device Nomenclature" figure
Section 4	Known Design Marginality/Exceptions to Functional Specifications: • Added "USB: Host Mode — Cannot Communicate With Low-Speed Device Through a Hub" advisory • Added "Master Subsystem MPU: Memory Protection Unit is Disabled" advisory • Added "Flash ECC: When Program/Data Cache is Enabled, ECC Errors are Captured Only on a Single 64-Bit Slice and Not on the Full 128-Bit Flash Bank Data Width" advisory • Added "Flash ECC: C28x 'Flash Uncorrectable' Error Generated When Executing F021 Flash API Functions With Flash ECC Enabled" advisory • Added "VREG: VREG 'Warn Lo/High' Feature Does Not Work as Intended" advisory • Added "Temperature Sensor: getTempSlope() and getTempOffset() Functions are not Available on TMX Silicon" advisory • Added "EMAC: Resetting EMAC Controller Using SRCR2 Register Does Not Automatically Reset the Ethernet PHY Via $\overline{\text{MII\_PHYRST}}$ Signal" advisory • Added "System Control: Clock Configuration Should Not be Changed When There are Pending/On-going Accesses to Shared RAM (Cx and Sx) or to Analog Subsystem" advisory • Added "RAM Controller: Cortex™-M3 Accesses to Shared RAM (Cx and Sx) and to MSG RAM Do Not Work When Any Other Master (µDMA/C28x/DMA) Simultaneously Accesses the Same Memory" advisory • Added "RAM Controller: µDMA Accesses to Shared RAM (Cx and Sx) and to MSG RAM Do Not Work When Any Other Master (Cortex™-M3/C28x/DMA) Simultaneously Accesses the Same Memory" advisory

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